AMENDMENTS TO THE CLAIMS

1 – 30. (canceled)

31. (currently amended) A method of forming a semiconductor device, said method comprising:

fabricating at least one electrical element on an upper side of a semiconductor substrate;

fabricating a plurality of bias voltage distribution regions over said upper side of said substrate for receiving a bias voltage and applying said bias voltage to said substrate; and

securing a conductive layer to a backside of said substrate, wherein said conductive layer is an electrical layer being adapted to receive an electric charge related to unwanted voltages and electrical noise from a first region of said substrate and return an electric charge to a second different region of said substrate to maintain a uniform bias voltage throughout the substrate.

32. (original) The method of claim 31, wherein said electrical element comprises at least one electrical element selected from the group consisting of transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

33. (original) The method of claim 31, wherein said conductive layer comprises a conductive metallic layer.

34. (original) The method of claim 33, said conductive metallic layer has a thickness of less than or equal to 10 mil.

35. (original) The method of claim 33, wherein said conductive metallic layer is secured to said substrate backside with a conductive adhesive.

36. (original) The method of claim 33, further comprising coupling said conductive metallic layer to a terminal for supplying said bias voltage.

37. (original) The method of claim 33, wherein said conductive metallic layer has a resisitivity less than between 1×10^{-8} Ohm-meter.

38. (currently amended) The method of claim 33, wherein said conductive metallic layer comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

39. (original) The method of claim 38, wherein said conductive metallic layer is formed of as least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

40. (original) The method of claim 33, wherein said conductive metallic layer has at least one length which exceeds a length of said substrate.

41. (original) The method of claim 33, wherein said conductive metallic layer is applied to said substrate back side after a fabricated wafer is cut into individual semiconductor devices.

42. (original) The method of claim 31, further comprises providing a plurality of conductive plugs for respectively coupling a received bias voltage source to said distribution regions.

43. (original) The method of claim 31, wherein said conductive layer comprises a cured conductive paste.

44. (original) The method of claim 43, wherein said conductive paste has a thickness less than or equal to 1 mil.

45. (original) The method of claim 43, wherein said conductive paste has a resistivity less than 1×10^{-5} Ohm-meter.

46. (original) The method of claim 43, wherein said conductive paste is formed of a material comprising conductive particles.

47. (original) The method of claim 43, wherein said conductive paste comprises conductive particles selected from at least one of the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

48. (original) The method of claim 43, further comprising applying said conductive paste to the backside of a fabricated wafer after the wafer is background and before the wafer is cut into individual semiconductor devices.

49. (original) The method of claim 31, wherein said conductive layer comprises an isotropically conductive polymeric film.

50. (original) The method of claim 49, wherein said conductive polymeric film has a thickness greater than about 1 mil.

51. (original) The method of claim 49, wherein said conductive polymeric film has a resistivity less than 1 x 10^{-5} Ohm-meter.

52. (original) The method of claim 49, wherein said conductive polymeric film comprises conductive particles selected from at least one of the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

53. (original) The method of claim 49, further comprising applying said conductive polymeric film to the backside of a fabricated wafer after said wafer is background and before said wafer is cut into individual semiconductor devices.

54. (original) The method of claim 49, wherein said conductive polymeric film is applied at a temperature greater than about 175 degrees Celsius.

55. (original) The method of claim 49, wherein said conductive polymeric film is pressed against said substrate at a pressure greater than 1 mega Pascal.

56. (original) The method of claim 31, wherein said conductive layer comprises a conductive metallic film.

57. (original) The method of claim 56, wherein said conductive metallic film has a thickness of less than or equal to 1 mil.

58. (original) The method of claim 56, wherein said conductive metallic film has a resistivity less than 1 x 10^{-5} Ohm-meter.

59. (original) The method of claim 56, wherein said conductive metallic film comprises conductive particles selected from at least one the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

60. (original) The method of claim 56, further comprising applying said conductive metallic film to the backside of a fabricated wafer after said wafer is background and before said wafer is cut into individual semiconductor devices.

61. (original) The method of claim 56, wherein said conductive metallic film is deposited by a method selected from the group consisting of: electroless plating, electrolytic plating, molecular beam epitaxy (MBE), vapor phase epitaxy (VPE), physical vapor deposition (PVD), chemical vapor deposition (CVD) and metal organic chemical vapor deposition (MOCVD).

62. (original) The method of claim 31, wherein said device is a memory device.

63. (original) The method of claim 62, wherein said memory device is a dynamic random access memory (DRAM) device.

64. (original) The method of claim 31, wherein said device is a logic device.

65. (original) The method of claim 31, wherein said device is a processor device.

66 – 99. (canceled)